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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/616,635 | 07/10/2003 | Michael Billeci | POU920030094US1 | 3411 |

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| EXAMINER | |
|---|---|
| MANOSKEY, JOSEPH D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2113 | |

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/616,635 | BILLECI ET AL. | |
| | Examiner | Art Unit | |
| | Joseph D. Manoskey | 2113 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Whalen, U.S. Patent 6,243,836.

3. Referring to claim 1, Whalen teaches tracing of a digital processor, this is interpreted as a method of capturing hardware trace data (See Col. 1, lines 5-11). Whalen teaches the use of trace buffer as a circular buffer, this is interpreted as defining a wrap-back address space (See Col. 4, lines 1-5). Whalen discloses wrap back of the trace buffer and compression of trace codes, this is interpreted as during compression mode, storing trace data circularly in the wrap-back address space (See Col. 6, lines 44-50). Whalen teaches storing the empty codes that are compressed into a 8-bit count of the number of 1s shifted into the register until the end of the sequence, this is interpreted as upon exiting compression mode, establishing a write address for further

trace data such that trace data prior to exiting compression mode is maintained (See Col. 7, lines 22-40).

4. Referring to claim 2, Whalen teaches reading the link of the beginning of the buffer and this address becomes the next start of the buffer, this is interpreted as said establishing said write address includes retrieving a jump-to address outside of said wrap-back address space and writing said further trace data to said jump-to address space (See Col. 8, lines 5-12).

5. Referring to claim 3, Whalen discloses incrementing a value of a start value for the buffer, this is interpreted as said establishing said write address includes incrementing a current write address within said wrap-back address space (See Col. 7, lines 6-21).

6. Referring to claim 4, Whalen teaches a status flag is set to indicate that the trace buffer wrapped, this is interpreted as said wrap-back address space holds N cycles of trace data; said storing trace data including maintaining a wrap-back flag that changes value every N cycles during compression (See Col. 10, lines 27-28).

7. Referring to claim 5, Whalen discloses when the wrapping of the trace buffer is detected a new start address is loaded for the buffer, this is interpreted as reordering

said trace data from said wrap-back address space in response to said wrap-back flag (See Col 7, lines 5-21).

8. Referring to claim 6, Whalen teaches including a target device that can be programmed such as a microcontroller and including an empty state, this is interpreted as providing a user programmable sensitivity setting for each unit generating trace data, each unit generating an idle signal in response to said sensitivity settings (See Col. 5, lines 1-32). Whalen also teaches compressing the empty codes, this is interpreted as entering said compression mode during which said trace data is compress upon a plurality of said units generating said idle signal (See Col. 7, lines 22-40).

9. Referring to claim 7, Whalen teaches tracing of a digital processor, this is interpreted as a system for capturing hardware trace data (See Col. 1, lines 5-11). Whalen teaches the use of trace buffer as a circular buffer, this is interpreted as trace arrays including a wrap-back address space (See Col. 4, lines 1-5). Whalen teaches a trace acquisition board with circular buffer controller, this is interpreted as trace controls including a trace data write address register containing an address within said trace arrays for trace data (See Fig. 1 and Col. 4, lines 43-60). Whalen also teaches monitoring the current trace buffer position and comparing it to the beginning of the buffer, this is interpreted as a wrap-back address decrementor (See Col. 7, line 66 to Col. 8, lines 1).

Whalen discloses wrap back of the trace buffer and compression of trace codes, this is interpreted as during compression mode, said trace controls controlling said address within said write address register by storing an output of said wrap-back address decrementor in said write address register to store trace data circularly in said wrap-back address space (See Col. 6, lines 44-50). Whalen teaches storing the empty codes that are compressed into a 8-bit count of the number of 1s shifted into the register until the end of the sequence, this is interpreted as upon exiting compression mode, said trace controls establishing said address within said write address register for further trace data such that trace data prior to exiting compression mode is maintained (See Col. 7, lines 22-40).

10. Referring to claim 8, Whalen teaches reading the link of the beginning of the buffer and this address becomes the next start of the buffer, this is interpreted as a jump-to address incrementor; said trace controls receiving a jump-to address from said jump-to address incrementor; said trace controls writing said jump-to address to said write address register, said further trace data being written to a jump-to address space (See Col. 8, lines 5-12).

11. Referring to claim 9, Whalen discloses incrementing a value of a start value for the buffer, this is interpreted as said an address incrementor; said trace controls receiving an incremented address from said address incrementor; said trace controls writing said incremented address to said write address register, said further trace data

being written to an incremented address space within said wrap-back address space (See Col. 7, lines 6-21).

12. Referring to claim 10, Whalen teaches a status flag is set to indicate that the trace buffer wrapped, this is interpreted as said wrap-back address space holds N cycles of trace data; said trace controls maintaining a wrap-back flag that changes value every N cycles during compression (See Col. 10, lines 27-28).

13. Referring to claim 11, Whalen discloses when the wrapping of the trace buffer is detected a new start address is loaded for the buffer, this is interpreted as said trace controls reorder said trace data from said wrap-back address space in response to said wrap-back flag (See Col 7, lines 5-21).

14. Referring to claim 12, Whalen teaches including a target device that can be programmed such as a microcontroller and including an empty state, this is interpreted as providing a user programmable sensitivity setting for each unit generating trace data, each unit generating an idle signal in response to said sensitivity settings (See Col. 5, lines 1-32). Whalen also teaches compressing the empty codes, this is interpreted as compression controls placing said trace controls in said compression mode during which said trace data is compressed upon a plurality of said units generating said idle signal (See Col. 7, lines 22-40).

15. Referring to claim 13, Whalen teaches including a target device that can be programmed such as a microcontroller and including an empty state, this is interpreted as a method of controlling compression of trace data in a processor, the method comprising providing a user programmable sensitivity setting for each unit generating trace data, each unit generating an idle signal in response to said sensitivity settings (See Col. 5, lines 1-32). Whalen also teaches compressing the empty codes, this is interpreted as entering a compression mode during which said trace data is compress upon a plurality of said units generating said idle signal (See Col. 7, lines 22-40).

16. Referring to claim 14, Whalen discloses starting the trace code, this is interpreted as said units generate a start signal initiating trace data capture (See Col. 8, lines 14-16). Whalen teaches compressing the empty codes when there has been more than three, this is interpreted as maintaining a count of cycles without receiving a start signal from one of said units and entering said compression mode when said count of cycles reaches a programmed limit (See Col. 7, lines 22-40).

17. Referring to claim 15, Whalen teaches compressing the empty codes until the end of the sequence is observed, this is interpreted as resetting said count of cycles to cease said compression mode when one of said units ceases generating said idle signal (See Col. 7, lines 22-40).

18. Referring to claim 16, Whalen teaches including a target device that can be programmed such as a microcontroller and including an empty state, this is interpreted as a system for controlling compression of trace data from units in a processor, the system comprising a user programmable sensitivity setting for each unit generating trace data, each said unit generating an idle signal in response to said sensitivity settings (See Col. 5, lines 1-32). Whalen also teaches compressing the empty codes, this is interpreted as compression controls generating a compression signal in response to a plurality of said units generating said idle signal and trace controls entering a compression mode in response to said compression signal, during which said trace data is compressed (See Col. 7, lines 22-40).

19. Referring to claim 17, Whalen discloses starting the trace code, this is interpreted as said units generate a start signal initiating trace data capture (See Col. 8, lines 14-16). Whalen teaches compressing the empty codes when there has been more than three, this is interpreted as said compression controls include a counter maintaining a count of cycles without receiving a start signal from one of said units and said compression controls generating said compression signal when said counter reaches a programmed limit (See Col. 7, lines 22-40).

20. Referring to claim 18, Whalen teaches compressing the empty codes until the end of the sequence is observed, this is interpreted as said counter resets to cease said

compression signal when one of said units ceases generating said idle signal (See Col. 7, lines 22-40).

21. Claims 19 and 20 are rejected under 35 U.S.C. 102(a) as being anticipated by Kahle et al., U.S. Patent 6,543,002, hereinafter referred to as "Kahle".

22. Referring to claim 19, Kahle teaches detecting hang which counts the number of cycles. A hang cycle register defines the maximum interval between assertions of completion valid signals that initiates a hang recovery sequence. Another register determines the interval between reject signal to the flush signal. This is interpreted as a method of pre-detecting a hardware hang in a processor, the method comprising: maintaining a count of a number of cycles in a predefined time interval without an instruction being completed; detecting a pre-hang condition if said count is within N counts of a hang limit; initiating trace capture in response to detecting said pre-hang condition; and detecting a hang condition if said count equals said hand limit (See Col. 7, line 1-21).

23. Referring to claim 20, Kahle teaches detecting hang which counts the number of cycles. A hang cycle register defines the maximum interval between assertions of completion valid signals that initiates a hang recovery sequence. Another register determines the interval between reject signal to the flush signal. This is interpreted as a system for pre-detecting a hardware hang in a processor, the system comprising: a

hang counter maintaining a count of a number of cycles in a predefined time interval without an instruction being completed; a pre-hang detector detecting a pre-hang condition if said hang counter is within N counts of a hang limit; a pre-hang detect latch initiating trace capture in response to said pre-hang detector detecting a pre-hang condition; and a hang detector resetting said pre-hang detect latch if said hang counter equals said hang limit (See Col. 7, line 1-21).

***Conclusion***

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Following are closely related trace systems.

U.S. Patent 6,839,869, to Doi et al.

U.S. Patent 6,985,848 to Swoboda et al.

U.S. Patent 7,039,834 to Orfali

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
November 20, 2006